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PAPER CODE	U375-294B (E&E)

(AY: 2025-26) December 2025 (ENDSEM) EXAM

TY E&TC (SEMESTER - I) (Pattern 2023)

COURSE NAME: System Design using Verilog Branch: E&TC COURSE CODE: ETUA31234B

Time: [1Hr 30 Min] **[Max. Marks: 40]**

(*) Instructions to candidates:

1) **Figures to the right indicate full marks. Use of scientific calculator is allowed.**
2) **Use suitable data wherever required.**
3) **All questions are compulsory. Solve any two sub question each from Questions 1 and 2.**
4) **Solve any one sub question (2 marks) from Questions 3, 4, 5 and 6 and sub question of 4 marks is compulsory from questions 3, 4, 5, and 6.**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	**a)** Design 4-to-1 Multiplexer using 2-to-1 multiplexers in Verilog.	[4]	CO1	[3]
	b) Design a 1-bit full subtractor in Verilog using dataflow modelling.	[4]	CO1	[3]
	c) Design 1-to-4 Demultiplexer in Verilog using behavioral modelling.	[4]	CO1	[3]
Q.2	**a)** Design D Flip-flop with asynchronous Set and Reset inputs in Verilog.	[4]	CO2	[3]
	b) Design an 8-bit DOWN counter with synchronous Reset in Verilog.	[4]	CO2	[3]
	c) Design 4-bit shift register to do Left shift operation in Verilog. Use asynchronous clear input to reset the data.	[4]	CO2	[3]
Q.3	**a)** What would be the output of the following statements? 1. latch = 4'hC; $display ("The current value of latch = %b", latch); 2. in_reg = 4'hC; $monitor ("In register value = %b", in_reg[2:0]); **OR**	[2]	CO3	[2]
	b) What will be the time period of the clock (clk) generated by the following code segment?	[2]	CO3	[2]

	`timescale 10ns/10ns module test_dut; initial clk = 1'b1; always forever begin #2.2 clk = 1'b0; #1.5 clk = 1'b1; end endmodule **c)** Draw the schematic of 2:1 CMOS multiplexer using CMOS switches and design it using Verilog.	[4]	CO3	[3]
Q.4	**a)** State any four features of XC9500 CPLD family. **OR** **b)** State any four features of XC4000E FPGA family. **c)** Construct optimized square look-up table for decimal numbers 0 to 7 using PROM.	[2] [2] [4]	CO4 CO4 CO4	[1] [1] [3]
Q.5	**a)** Draw the data path diagram to do GCD computation. **OR** **b)** Draw the data path diagram to do multiplication by repeated addition. **c)** Design a sequence detector using Verilog to detect a nonoverlapping sequence "1011" using Moore FSM. Draw state diagram and write a design code.	[2] [2] [4]	CO5 CO5 CO5	[2] [2] [3]
Q.6	**a)** List the step-wise micro-instructions required to execute instruction ADDI R2, R5, 150. **OR** **b)** List the step-wise micro-instructions required to execute instruction LW R2, 200 (R6). **c)** Consider a pipeline that carries out the following stage-wise operations: **Inputs:** Three register addresses (rs1, rs2 and rd), an ALU function (func), and a memory address (addr). **Stage 1:** Read two 16-bit numbers from the registers specified by "rs1" and "rs2", and store them in A and B. **Stage 2:** Perform an ALU operation on A and B specified by "func", and store it in Z. **Stage 3:** Write the value of Z in the register specified by "rd". **Stage 4:** Also write the value of Z in memory location "addr". Construct a pipelined architecture to perform above operations.	[2] [2] [4]	CO6 CO6 CO6	[2] [2] [3]